IN THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application.

1. (Original) A semiconductor integrated circuit device comprising:

a first wiring extending in a first direction;

a second wiring extending in a second direction crossing the first direction; and

a magnetoresistive effect device including a first magnetic layer, nonmagnetic layer, and second magnetic layer, wherein

the planar shape of the magnetoresistive effect device coincides with the planar shape of the crossing portion between the first wiring and the second wiring.

2. (Withdrawn) The device according to claim 1, wherein a contact with the first wiring is present on the lower face of the magnetoresistive effect device and a contact with the second wiring is present on the upper face of the magnetoresistive effect device.

3. (Original) The device according to claim 2, wherein the magnetoresistive effect device is stacked with a rectifying device.

4. (Original) The device according to claim 1, further comprising:

a third wiring extending in the second direction and formed in parallel with the second wiring through a gap, wherein the contact with the first wiring is present on the lower face of the magnetoresistive effect device and the contact with the third wiring is present on the upper face of the magnetoresistive effect device.

5. (Withdrawn) The device according to claim 1, wherein a contact with the first wiring is present on the lower face of the magnetoresistive effect device and the upper face of the magnetoresistive effect device connects with one end of a lead electrode and the other end of the lead electrode connects with the source or drain diffusion layer of a MOSFET.

6. (Original) A semiconductor integrated circuit device comprising:

a first wiring extending in a first direction;

a second wiring extending in a second direction crossing the first direction; and

a magnetoresistive effect device including a first magnetic layer, nonmagnetic layer, and second magnetic layer, wherein the magnetoresistive effect device is a magnetoresistive effect device constituted by a magnetic recording layer including a magnetic layer, a tunnel blocking layer including a nonmagnetic layer, and a magnetized fixed layer including a magnetic layer, wherein the planar shape of the magnetic recording layer coincides with the planar shape of the crossing portion between the first wiring and the second wiring and the planar shape of the magnetized fixed layer coincides with the planar shape of the first wiring.

7. (Withdrawn) A method of manufacturing a semiconductor integrated circuit device, comprising:

forming a first insulating layer on a semiconductor substrate;

forming a first conductive layer on the first insulating layer;

forming a magnetoresistive effect device layer including at least a first magnetic layer, nonmagnetic layer, and second magnetic layer on the first conductive layer;

working the magnetoresistive effect device layer and the first conductive layer by using a mask corresponding to a first wiring pattern;

forming a second insulating layer on the worked magnetoresistive effect device layer and the first insulating layer;

planarizing the second insulating layer so that the upper face of the second insulating layer and the upper face of the magnetoresistive effect device layer are exposed on the same plane;

forming a second conductive layer on the second insulating layer and the magnetoresistive effect device layer; and

working the second conductive layer and the magnetoresistive effect device layer by using a mask having a pattern corresponding to a second wiring pattern.

8. (Withdrawn) The method according to claim 7, wherein when working the magnetoresistive effect device layer, only either of the first magnetic layer and the second magnetic layer is worked to stop working at the nonmagnetic layer.

9. (Withdrawn) The method according to claim 8, wherein the magnetoresistive effect device layer is a TMR layer including a magnetic recording layer, tunnel blocking layer, and magnetized fixed layer and when working the magnetoresistive effect device layer, the magnetic recording layer is worked and working is stopped at the tunnel blocking layer.

10. (Withdrawn) A method of manufacturing a semiconductor integrated circuit device, comprising:

forming a first insulating layer on a semiconductor substrate;

forming a first conductive layer on the first insulating layer;

forming a composite layer including a rectifying device layer and a magnetoresistive effect device layer formed by at least a first magnetic layer, nonmagnetic layer, and second magnetic layer on the first conductive layer;

working the composite layer and the first conductive layer by using a mask having a pattern corresponding to a first wiring pattern;

forming a second insulating layer on the first pattern and the first insulating layer;

planarizing the second insulating layer so that the upper face of the second insulating layer and the upper face of the composite layer are exposed on the same plane;

forming a second conductive layer on the second insulating layer and the composite layer; and

working the second conductive layer and the composite layer by using a mask having a pattern corresponding to a second wiring pattern.

11. (Withdrawn) The method according to claim 10, wherein when working the composite layer, only either of the first magnetic layer and the second magnetic layer is worked to stop working at the nonmagnetic layer.

12. (Withdrawn) The method according to claim 11, wherein the magnetoresistive effect device layer included in the composite layer is a TMR including a magnetic recording layer, tunnel blocking layer, and magnetized fixed layer and when working the magnetoresistive effect device layer, the magnetic recording layer is worked to stop working at the tunnel blocking layer.

13. (Original) A method of manufacturing a semiconductor integrated circuit device, comprising:

forming a first insulating layer on a semiconductor substrate;

forming a first conductive layer on the first insulating layer;

forming a magnetoresistive effect device layer including at least a first magnetic layer, nonmagnetic layer, and second magnetic layer on the first conductive layer;

working the magnetoresistive effect device layer and the first conductive layer by using a mask having a pattern corresponding to a first wiring pattern;

forming a second insulating layer on the worked magnetoresistive effect device layer and the first insulating layer;

planarizing the second insulating layer so that the upper face of the second insulating layer and the upper face of the magnetoresistive effect device layer are exposed on the same plane;

forming a second conductive layer on the second insulating layer and the TMR layer;

forming a third insulating layer on the second conductive layer;

forming a third conductive layer on the third insulating layer; and

working the third conductive layer, the third insulating layer, the second conductive layer, and the magnetoresistive effect device layer by using a mask having a pattern corresponding to a second wiring pattern.

14. (Original) The method according to claim 13, wherein when working the magnetoresistive effect device layer, only either of the first magnetic layer and the second magnetic layer is worked to stop working at the nonmagnetic layer.

15. (Original) The method according to claim 14, wherein the magnetoresistive effect device layer is a TMR layer including a magnetic recording layer, tunnel blocking layer, and

magnetized fixed layer and when working the magnetoresistive effect device layer, the magnetic recording layer is worked and working is stopped at the tunnel blocking layer.

16. (Original) A method of manufacturing a semiconductor integrated circuit device, comprising:

forming a first insulating layer on a semiconductor substrate;

forming a first conductive layer on the first insulating layer;

forming a composite layer including a rectifying device layer and a magnetoresistive effect device layer formed by at least a first magnetic layer, nonmagnetic layer, and second magnetic layer on the first conductive layer;

working the composite layer and the first conductive layer by using a mask having a pattern corresponding to a first wiring pattern;

forming a second insulating layer on the worked composite layer and the first insulating layer;

planarizing the second insulating layer so that the upper face of the second insulating layer and the upper face of the composite layer are exposed on the same plane;

forming a second conductive layer on the second insulating layer and the magnetoresistive effect device layer;

forming a third insulating layer on the second conductive layer;

forming a third conductive layer on the third insulating layer; and

working the third conductive layer, the third insulating layer, the second conductive layer, and the composite layer by using a mask having a pattern corresponding to a second wiring pattern.

17. (Currently amended) The method according to claim [[13]] 16, wherein when working the composite layer, only either of the first magnetic layer and the second magnetic layer is worked to stop working at the nonmagnetic layer.

18. (Currently amended) The method according to claim [[14]] 17, wherein the magnetoresistive effect device layer included in the composite layer is a TMR including a magnetic recording layer, tunnel blocking layer, and magnetized fixed layer and when working the magnetoresistive effect device layer, the magnetic recording layer is worked to stop working at the tunnel blocking layer.

19. (Original) A method of manufacturing a semiconductor integrated circuit device, comprising:

forming a first insulating layer on a semiconductor substrate on which an insulating-gate-type field-effect transistor is formed;

planarizing the first insulating layer;

forming a first conductive layer on the first insulating layer;

forming a magnetoresistive effect device layer including at least a first magnetic layer, nonmagnetic layer, and second magnetic layer on the first conductively layer;

working the magnetoresistive effect device layer and the first conductive layer by using a mask having a pattern corresponding to a first wiring pattern;

forming a second insulating layer on the worked magnetoresistive effect device layer and the first insulating layer;

planarizing the second insulating layer so that the upper face of the second insulating layer and the upper face of the magnetoresistive effect device layer are exposed on the same plane;

forming a via to be electrically connected to the source or drain of the insulating-gate-type field-effect transistor by penetrating the second insulating layer and the first insulating layer;

forming a second conductive layer on the second insulating layer and the magnetoresistive effect device layer;

working the second conductive layer into a pattern contacting with the magnetoresistive effect device and the via;

forming a third insulating layer on the worked second conductive layer and the second insulating layer;

forming a third conductive layer on the third insulating layer; and

working the third conductive layer, the third insulating layer, the second conductive layer, and the magnetoresistive effect device layer by using a mask having a pattern corresponding to a second wiring pattern.

20. (Original) The method according to claim 19, wherein when working the magnetoresistive effect device layer, only either of the first magnetic layer and the second magnetic layer is worked to stop working at the nonmagnetic layer.

21. (Original) The method according to claim 20, wherein the magnetoresistive effect device layer is a TMR layer including a magnetic recording layer, tunnel blocking layer, and magnetized fixed layer and when working the magnetoresistive effect device layer, the magnetic recording layer is worked and working is stopped at the tunnel blocking layer.

22. (New) The device according to claim 3, further comprising:

a third wiring extending in the second direction and formed in parallel with the second wiring through a gap, wherein the contact with the first wiring is present on the lower face or the upper face of the magnetoresistive effect device and the contact with the third wiring is present on the upper face or the lower face of the rectifying device.